Using the HI1176/HI1179 Evaluation Board

Author: Bob Huckabee

Description

The HI1176/HI1179 evaluation board can be used to evaluate the performance of the HI1176 (8-bit, 20MSPS) and the HI1179 (8-bit, 35 MSPS) analog-to-digital converters (ADC). The board includes clock driver circuitry, an external reference voltage generator, data output buffer, and a digital to analog converter (DAC).

The HI1176 and the HI1179 are 8-bit CMOS 2-step A/D converters designed in 1.4µm and 1.0µm CMOS processes, respectively. These parts are pin for pin compatible with differences being the maximum guaranteed clock speed (20MSPS vs 35MSPS) and the HI1176 has a built in monostable multivibrator where the HI1179 does not (See Table 1). The evaluation board is built to be used for both the HI1176 and the HI1179, therefore the monostable multivibrator on the HI1176 is not utilized but it is discussed.

The HI1171 (8-bit, 40MHz) DAC is used to reconstruct the HI1176/HI1179 digital outputs, allowing the user to see the results of a “complete” 8-bit system. Refer to Table 2 for more specifications on the HI1171.

HI1176/1179 Theory of Operation

As illustrated in the functional block diagram, Figure 2, of the HI1176/HI1179, the part is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can be obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type CMOS comparator that operates synchronously with the external clock. The operating modes of the part are input sampling (S), hold (H), and compare (C). This design requires fewer comparators than typical flash converters thereby lowering the power dissipation.

The operation of the part is depicted in the timing diagram of Figure 3. A reference voltage between V_{RT} and V_{RB} is constantly applied to the upper 4-bit comparator group. The analog input is sampled, $V_I(1)$, with the falling edge of the first clock by the upper comparator group. The lower block A also samples the analog input, $V_I(1)$, on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 cycle clock delay from the analog input sampling point to the corresponding digital output data. The lower comparator blocks A and B alternate generating the lower data in order to increase the overall ADC sampling rate.

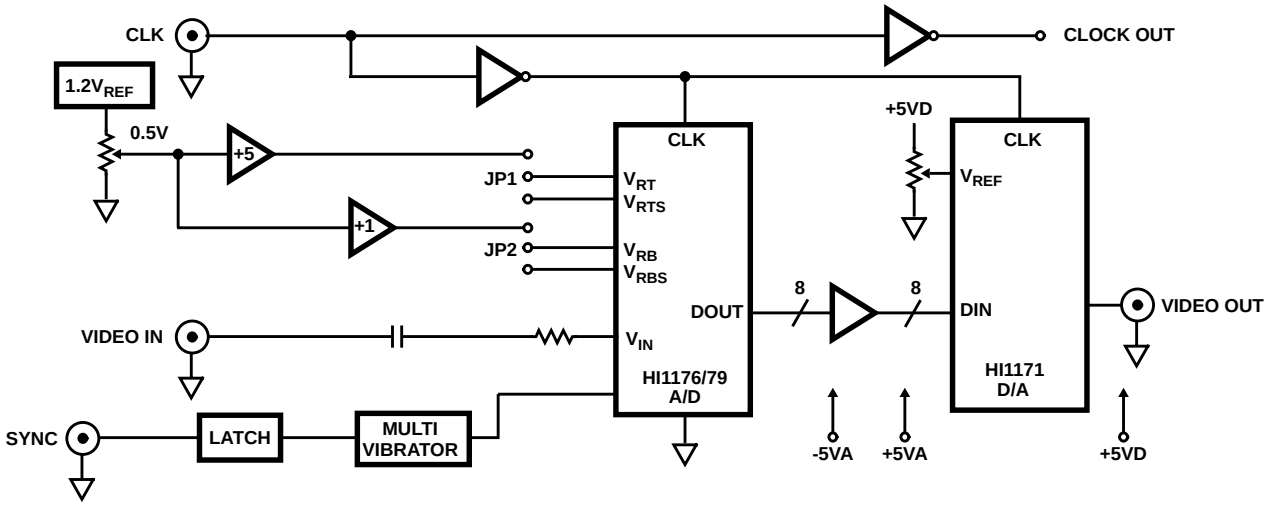
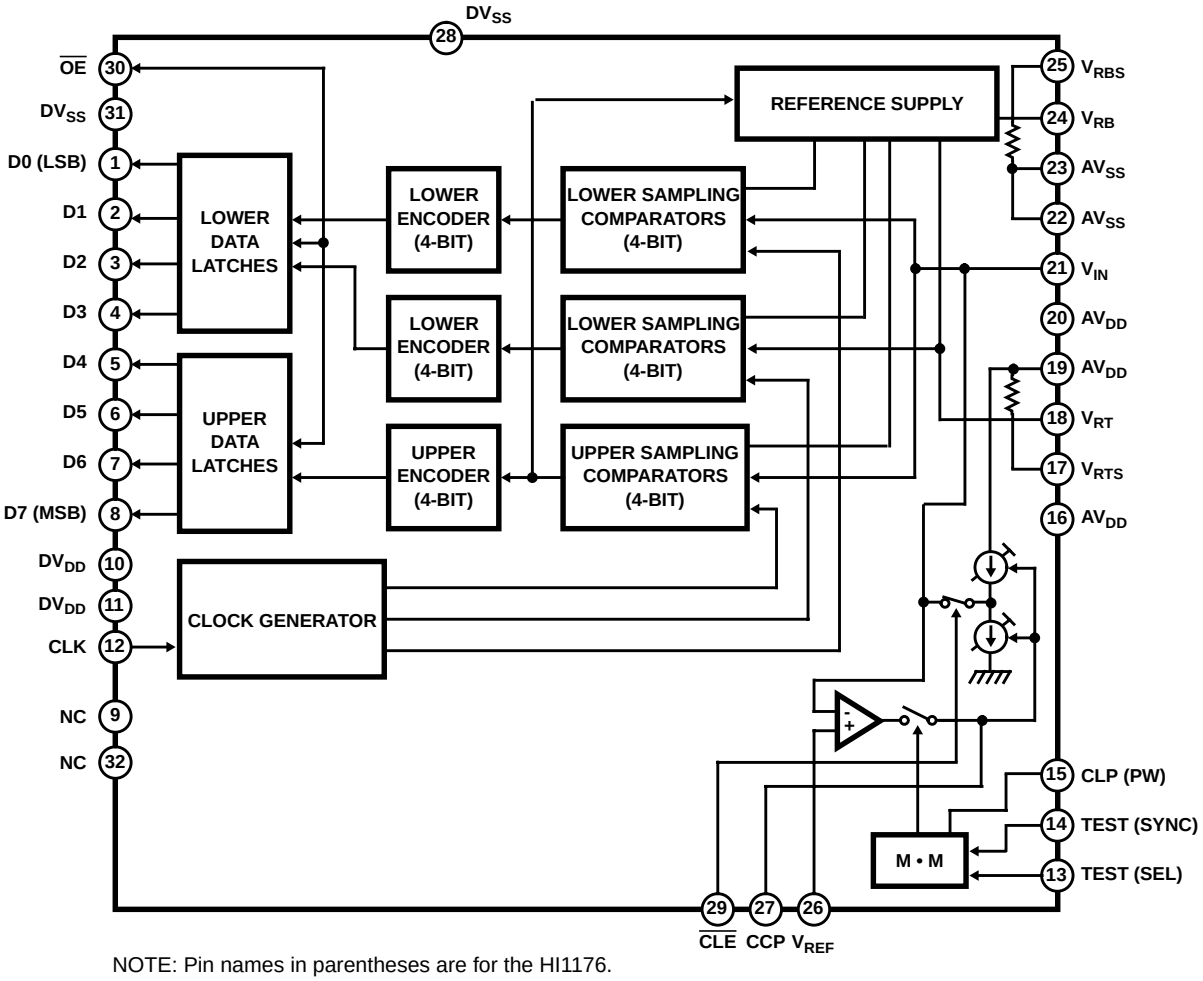


FIGURE 1. EVALUATION BOARD BLOCK DIAGRAM

Copyright © Intersil Corporation 1994

TABLE 1. HI1176/HI1179 PIN FOR PIN DIFFERENCES

PIN	HI1176 NAME	HI1179 NAME	HI1176 PIN DESCRIPTION	HI1179 PIN DESCRIPTION
13	SEL	TEST	SEL determines what edge the monostable multivibrator is triggered on. Low: falling edge. High: rising edge.	Set to V_{DD} or V_{SS}. For Test Purposes Only.
14	SYNC	TEST	SYNC is the trigger pulse input to the monostable. Trigger polarity is controlled by pin 13 (SEL).	Set to V_{DD} or V_{SS}. For Test Purposes Only.
15	PW	CLP	When a clamp pulse is generated by the monostable multivibrator, the pulse width is determined by an external R and C connected to pin 15. When the clamp pulse is inputted directly, it is connected to pin 15 (PW).	Clamp pulse input. The analog input is clamped to V_{REF} while the clamp pulse is low.



NOTE: Pin names in parentheses are for the HI1176.

FIGURE 2. HI1176/HI1179 FUNCTIONAL BLOCK DIAGRAM

TABLE 2. HI1171 DATASHEET SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
Throughput Rate	40	-	-	MSPS
INL	-0.5	-	1.3	LSB
DNL	-0.25	-	+0.25	LSB
Voltage Reference Input Range	0.5	-	2.0	V
Full Scale Output Current	-	10	15	mA
Differential Gain	-	1.2	-	%
Differential Phase	-	0.5	-	Degree

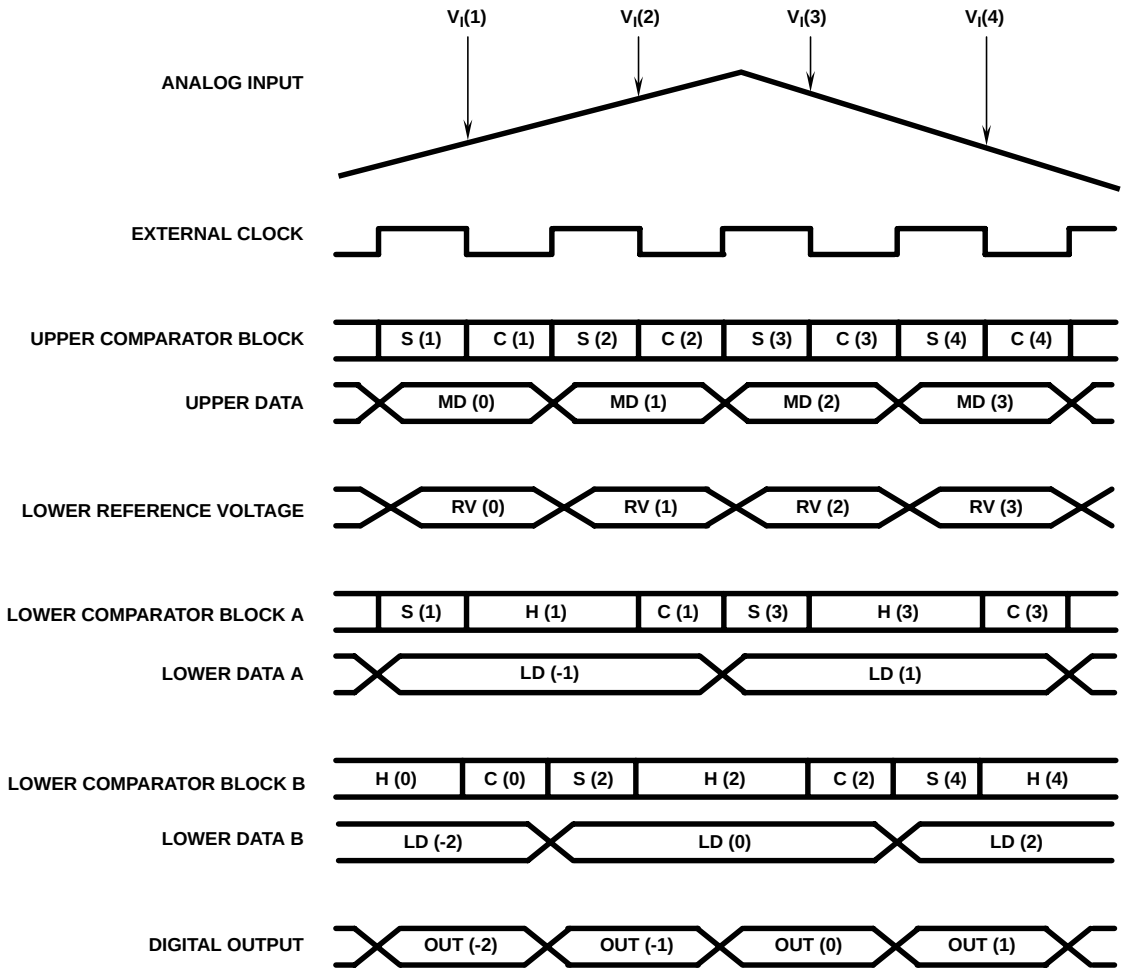


FIGURE 3. HI1176/HI1179 TIMING

Layout and Power Supplies

The HI1176/HI1179 evaluation board is a four layer board with a layout optimized for the best performance for the ADC. The two internal layers are power and ground with the analog and digital planes separated. The ground planes are connected at one point (JP9) near the ADC. Figure 9 through Figure 16 include a schematic of the board, a board layout, and the various board layers. The user should feel free to copy any part of the layout for their application.

In order to optimize performance of the HI1176/HI1179 at power up, AV_{DD} and DV_{DD} are driven from separate supplies. The supplies to the board should be driven by individual clean linear regulated supplies. They can be hooked up with external 16 gauge wires to the holes marked +5VD, +5VA, -5VA, DGND, and AGND on the prototype area. Do not tie the supply grounds together back at the supplies as this will create a ground loop and create additional noise.

The analog and digital supplies can be sequenced in any order. There is no concern about latch-up for the HI1176 or HI1179. The HI1171 does require the positive supply to power up first, but no sequencing problems have been observer with the evaluation board.

If only one +5V supply is desired for the analog and digital power then apply +5V at +5VA and install JP9. This will connect the analog power to the digital power through a ferrite bead (see schematic). No real difference in room temperature performance has been observed when using either supply connection.

The operating conditions for the power supplies are listed below.

TABLE 3. POWER SUPPLY REQUIREMENTS

POWER SUPPLY	MIN	TYP	MAX	TYP CURRENT
+5VD	+4.75V	+5.0V	+5.25V	80mA
+5VA	-	+5.0V	-	40mA
-5VA	-	-5.0V	-	8mA

Reference Circuit

For the following discussion, refer to the board schematic and the board layout drawing.

The HI1176/HI1179 requires two reference voltages: V_{RT} and V_{RB}. The evaluation board provides the user with two options for supplying these voltages. First, by setting jumpers JP1 and JP2 to INT, the internal bias generators on the part can be used to generate a V_{RT} of about 2.6V and a V_{RB} of about 0.6V. These generators are resistors to V_{DD} and V_{SS} which in combination with the internal reference resistor string generates the desired voltages. The absolute value of V_{RT} and V_{RB} can vary from part to part due to offsets (see datasheet), but the voltages are stable over temperature. This is the simplest and cheapest method but power supply variations and noise may be directly coupled into the reference. The noise can be minimized with good supply and reference decoupling.

The evaluation board also provides an external reference that can be applied to the part by setting jumpers JP1 and JP2 to EXT. In this case an ICL8069 reference diode generates a voltage, 1.2V, that is gained up by two op-amps to the reference voltages: V_{RT} and V_{RB}. V_{RB} is set to 0.5V ±2mV by adjusting P1 then P2 is adjusted for a V_{RT} reference voltage of +2.5V ±2mV. The HI1176/HI1179 has the best performance when V_{RT} - V_{RB} is kept above 1.8V and less than 2.8V, and V_{RT} is kept below 2.8V. An external reference may provide the best reference depending on the application, at the expense of board space and cost.

No real difference in room temperature performance has been observed when using either the internal or external reference on the evaluation board.

Analog Input

The analog input to the HI1176/HI1179 can be configured in various ways depending on the input signal and the required level of performance. Due to the low input capacitance an input buffer is not necessary, but the input should be driven from a low impedance source. The evaluation board does allow for a transistor buffer if the user so desires, but it is not connected.

A signal voltage with a maximum span of V_{RT} - V_{RB} can be AC coupled to the HI1176/HI1179 through the V_{IN} BNC and applied to the ADC. This is necessary if using the internal DC restore (input clamp). If the DC restore function is not being used then the input can be DC coupled and offset between V_{RT} and V_{RB}. If the input is AC coupled with the clamp function disabled, the input signal will go to about $1/2(V_{RT} + V_{RB})$.

Input Clamp

The HI1176 and the HI1179 have the capability to clamp the input signal before it is digitized by the ADC, see Figure 8. A comparator is used to determine if the input, during the clamp pulse time, is above or below the desired clamp voltage, V_{REF}. The appropriate current source will be turned on to charge the input capacitor up or down depending on the comparator output. The HI1176 has an internal monostable multivibrator that can be set to run in various modes of clamp pulse operation. For example, if performing the DC restore function for NTSC video, the HI1176/HI1179 can be configured to clamp the back porch of the incoming video to the voltage on the V_{REF} pin. If a sync detect function is required after the ADC, then V_{REF} can be set so the complete video signal including the sync pulse is digitized. If the sync is to be stripped before the ADC then V_{REF} can be set so only the active video portion of the video gets digitized. This will effectively increase the resolution for this portion of the video signal.

The evaluation board has the SYNC pulse input latched by the ADC sampling clock and is connected to the PW (CLP for the HI1179) input. This is done to prevent beat frequencies, generated between the clock and clamp inputs, from showing up as vertical sag in video applications. If this is not a concern the latch is not necessary.

The clamp reference voltage, V_{REF}, is set by P7 and is adjusted to 1.0V at the factory.

There are several methods for implementing the input DC restore function when using the HI1176. One method is to directly input the clamp pulse as is done on the evaluation board. Another method is to use the internal monostable multivibrator, eliminating the external monostable multivibrator. To use the built in multivibrator an RC network is necessary to set the pulse width on pin 15 and the clamping pulse is connected to pin 14 (SYNC). An RC of 130k and 100pF gives a 2.75µs pulse. Narrower pulse widths can be achieved by reducing the resistor value. The SEL pin (pin 13) will determine which SYNC edge the pulse is generated on.

Output Enable Input

The output enable input, $\overline{OE}$, when held low, enables the digital outputs. When held high, the digital outputs are tri-stated. (See Figure 4.) The $\overline{OE}$ input on the evaluation board is tied to ground through a 50 ohm resistor and is connected to the 50 pin connector. This keeps the output enabled and allows the users to test the $\overline{OE}$ pin by connecting a pulse generator to the $\overline{OE}$ pin on the 50 pin connector. Typical enable/disable times are listed in Table 4.

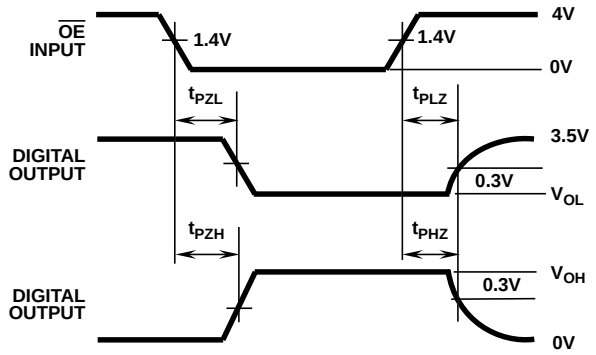


FIGURE 4. ENABLE/DISABLE TIMING

TABLE 4. OUTPUT ENABLE/DISABLE TIMES

PART	t_{PZL}	t_{PLZ}	t_{PZH}	t_{PHZ}	UNITS
HI1176	7.4	7.6	8.0	8.0	ns
HI1179	5.0	6.0	5.4	5.6	ns

DAC Setup

The DAC output fullscale is adjusted by P6 and is set to 1V.

The internal latch is closed when the clock line is high. The latch can be cleared by the BLNK line. When BLNK is set high, the contents of the internal data latch will be cleared. When BLNK is low, data is updated by the clock.

The references are set to give a 1V full scale output into 75Ω. The 75Ω is assumed to be at the terminating end of a piece of coax. The evaluation board has resistor options for a terminating resistor and a series resistor if so required. The output current and voltage can be set by the user and is determined as follows for the evaluation board:

$$_{REF} = V_{REF}/R_{REF} = 1V/1.2k = 0.833mA$$

$$_{OUT} = I_{REF} \times 16 = 0.833mA \times 16 = 13.33mA$$

$$_{OUT} = I_{OUT} \times R_{OUT} = 13.33mA \times 75 = 1V$$

As the values of R_{OUT} and R_{REF} increase power dissipation decreases, but glitch energy and output settling time increase as well as differential gain and phase.

Increased Accuracy

Further calibration of the ADC can be done when using the external reference and input buffer circuit. First, a precision voltage equal to the ideal V_{IN-FS} + 0.5 LSB is applied at V_{IN1}. P1 is then adjusted until the 0 to 1 transition occurs on the digital output. Finally, a voltage equal to the ideal V_{IN+FS} - 1.5 LSB is applied at V_{IN1}. P2 is then adjusted until the 254 to 255 transition occurs on the digital output.

Input Clock Driver and Timing

The input clock to the HI1176/HI1179 evaluation board is a standard TTL or CMOS clock applied to the CLOCK INPUT BNC. U4 (75ACT04) will buffer the clock and convert it to the CMOS levels necessary to drive the HI1176/HI1179. For optimum performance of the HI1176/HI1179 the duty cycle of the clock should be kept at 50% ± 10%.

U5 (74ACT541) acts as a buffer for the digital outputs.

Figure 5 shows the timing for the evaluation board. The data corresponding to a particular sample will be available at the output of the HI1176/HI1179 after the required data latency (2.5 cycles) plus an output delay. Table 5 lists the values that can be expected for the various timing delays. Refer to the datasheet for additional timing information

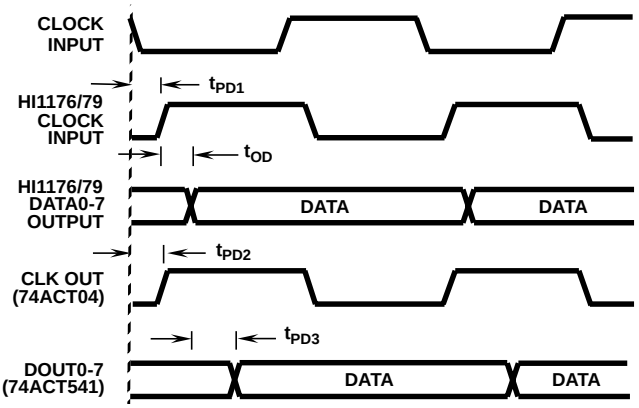


FIGURE 5. INPUT-TO-OUTPUT TIMING

TABLE 5. EVALUATION BOARD TIMING

PARAMETER	DESCRIPTION	MIN	TYP	MAX
t_{OD}	Data Delay HI1176	-	18ns	30ns
	Data Delay HI1179	7ns	13ns	18ns
t_{PD1}	74ACT04 Prop Delay	2.4ns	-	8.5ns
t_{PD2}	74ACT04 Prop Delay	2.4ns	-	8.5ns
t_{PD3}	74ACT541 Prop Delay	2.1ns	-	7.5ns
t_S	HI1171 Setup Time	10ns	-	-
t_H	HI1171 Hold Time	2ns	-	-
t_{PD}	HI1171 Data Delay	-	10ns	-

HI1176/HI1179 Characterization

Various tests can be used to characterize the performance of the HI1176/HI1179. The integral nonlinearity (INL) and differential nonlinearity (DNL) specs are considered a measure of the low frequency characteristics of the ADC. These parameters are evaluated at the factory using a histogram approach with a low frequency ramp input.

Further dynamic testing is used to evaluate the HI1176/HI1179 performance as the input starts to approach nyquist ($F_S/2$). Among these tests are Signal-to-Noise Ratio (SNR), Signal-to-Noise And Distortion (SINAD), and Total Harmonic Distortion (THD).

Coherent testing is recommended in order to avoid the inaccuracies due to windowing. Coherent sampling is governed by the following relationship: $F_T/F_S = M/N$, where F_T is the frequency of the input tone, F_S is the sampling frequency, N is the number of samples, and M is the number of cycles over which the samples are taken. By making M an integer and prime (1, 3, 5...) the samples are assured of being non-repetitive.

Figure 6 shows the test system used to do dynamic testing on the HI1176/HI1179. The clock (CLK) and analog input (AIN) signal sources are derived from low phase noise HP8662A generators that are phase locked to each other to ensure coherence. The output of the generator that drives the analog input to the evaluation board is first passed through a bandpass filter to improve the spectral purity of the signal. The ADC data is captured by a logic analyzer and then transferred over the GPIB bus to the PC. The PC has all the software to perform the Fast Fourier (FFT) and do the required data analysis.

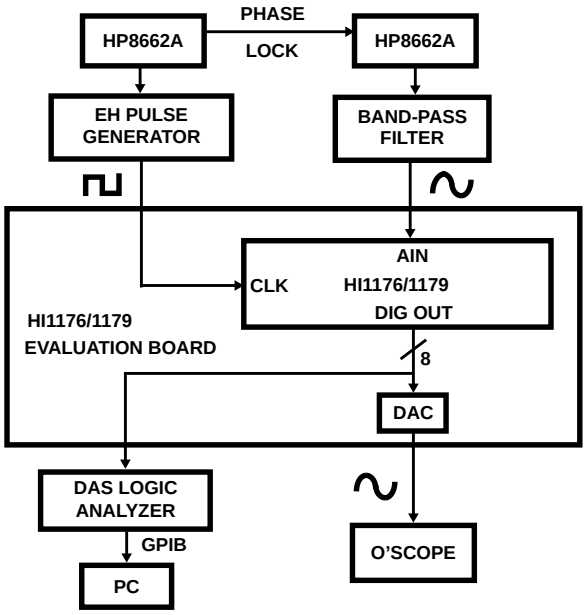


FIGURE 6. COHERENT TEST SYSTEM

Bandwidth

A 12-bit accurate DAC is used to do the bandwidth testing. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The CLK and analog input frequencies are set up so a 1kHz beat frequency is generated on the output of the DAC. Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output is 3dB down from the low frequency value.

Video Testing

To characterize the HI1176/HI1179 for NTSC video performance the test setup in Figure 7 was used.

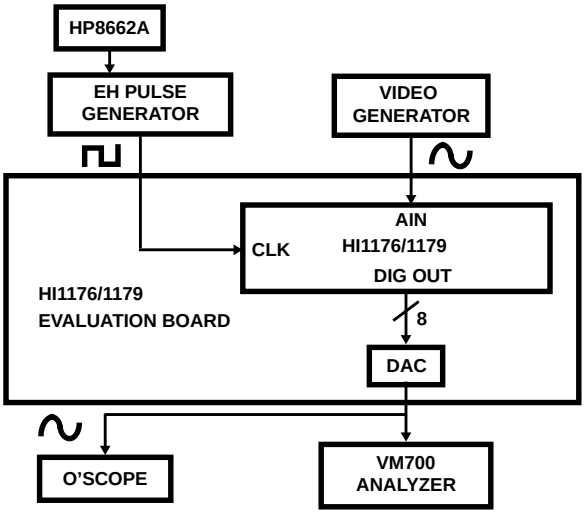


FIGURE 7. VIDEO TEST SYSTEM

The differential gain (DG) and differential phase (DP) measurements are listed in Table 6. The measurements are made at the output of the HI1171, this includes A/D and D/A performance. The HI1171 was terminated into 75Ω. DP and DG increase as R_{OUT} increases for the HI1171.

TABLE 6. VIDEO PERFORMANCE

	HI1176		HI1179	
f_{CLK}	DG	DP	DG	DP
14.32MHz	0.5	0.9	-	-
20.0MHz	0.6	0.9	0.8	0.5
28.64MHz	-	-	0.6	0.7

Acknowledgments

Thanks to Phil Louzon and Gary Smith for their technical assistance.

References

AN8906, "Noise Aspects of Applying Advanced CMOS Semiconductors."

AN9102, "Noise Aspect of Applying Advance CMOS Semiconductors."

AN9214.2, "Using Intersil High Speed A/D Converters."

AN9313.1, "Circuit Considerations in Imaging Applications."

Michael O. Felix, "Differential Phase and Gain Measurements in Digitized Video Signals", SMPTE Journal, 85:76-79,February 1976.

Frederick A. Williams and Richard K. Olsen, "Quantization Effects on Differential Phase and Gain Measurements", SMPTE, Nov. 1982.

W. D. Bartlett, "Quantization Effects When Testing Differential Gain", IMTC, 366-368, May 1992.

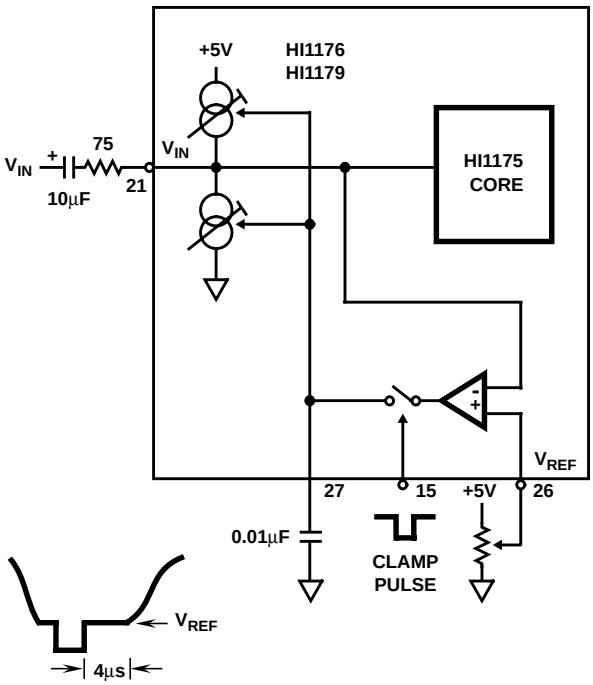


FIGURE 8. CLAMP BLOCK DIAGRAM

TABLE 7. FACTORY BOARD SETTING

JP1	V_{RT}, Set for internal reference
JP2	V_{RB}, Set for internal reference
JP3	$\overline{CLE}$, Set low, input clamp function is enabled.
JP4	SEL, Set low, the falling edge of pin 14 will trigger the monostable on the HI1176. It is a do not care for the HI1179.
JP5	BLK_IN, Set low, HI1171 Blanking is off.
JP6	Selects edge to trigger on for input clamp. Set to trigger on falling edge, Q. Selecting $\overline{Q}$ will set clamp to trigger on the rising edge.
JP9	+5V supply, jumper is installed. Only one +5V supply is required with jumper installed. Remove if separate analog and digital supplies are to be used.
P1	Set to give 0.5V at V_{RB} EXT jumper pin.
P2	Set to give 2.5V at V_{RT} EXT jumper pin.
P4	Set to 2.5V, DC offset for Clock Input.
P6	Set to 1.0V, HI1171 V_{REF}.
P7	Set to 1.0V, Clamp V_{REF}.

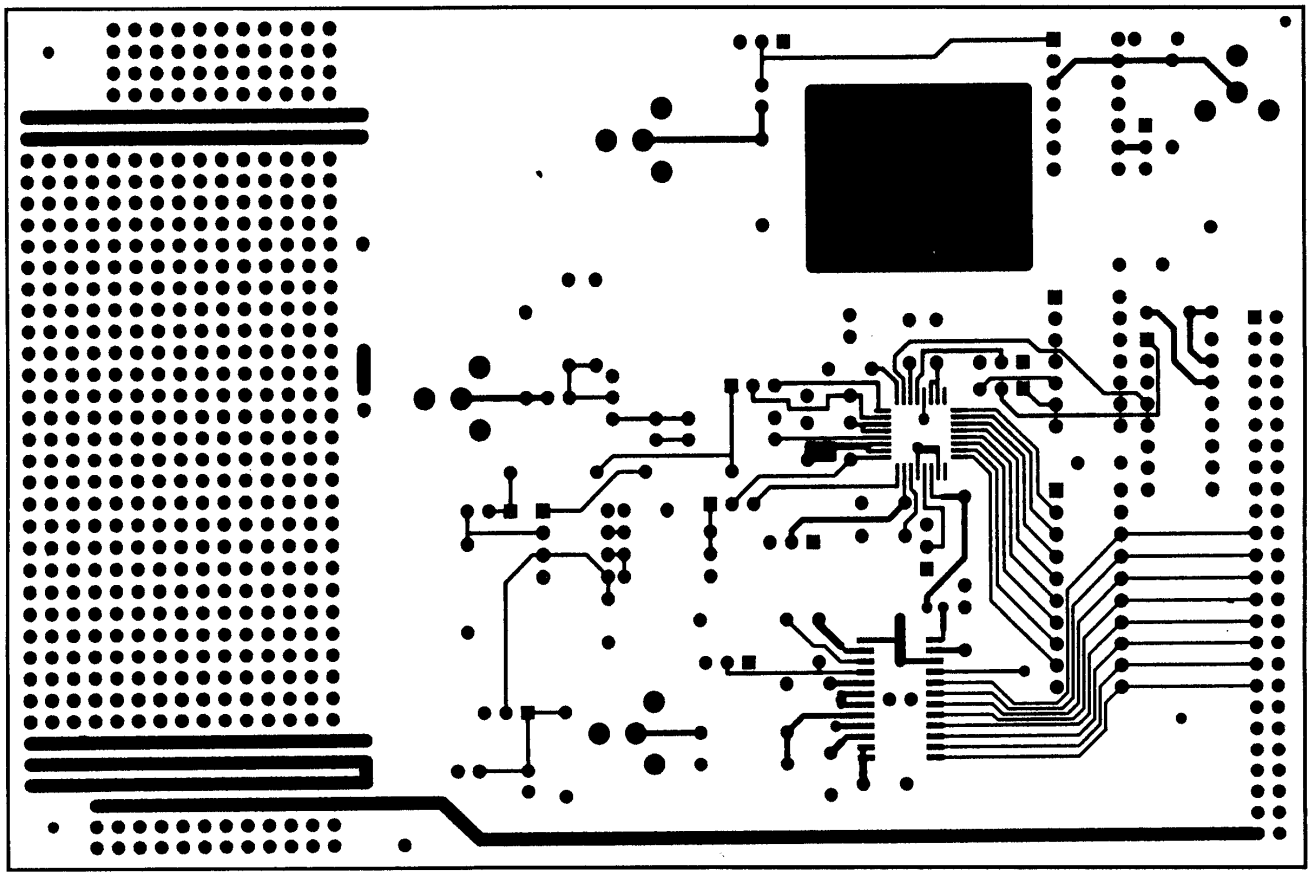


FIGURE 9. COMPONENT SIDE

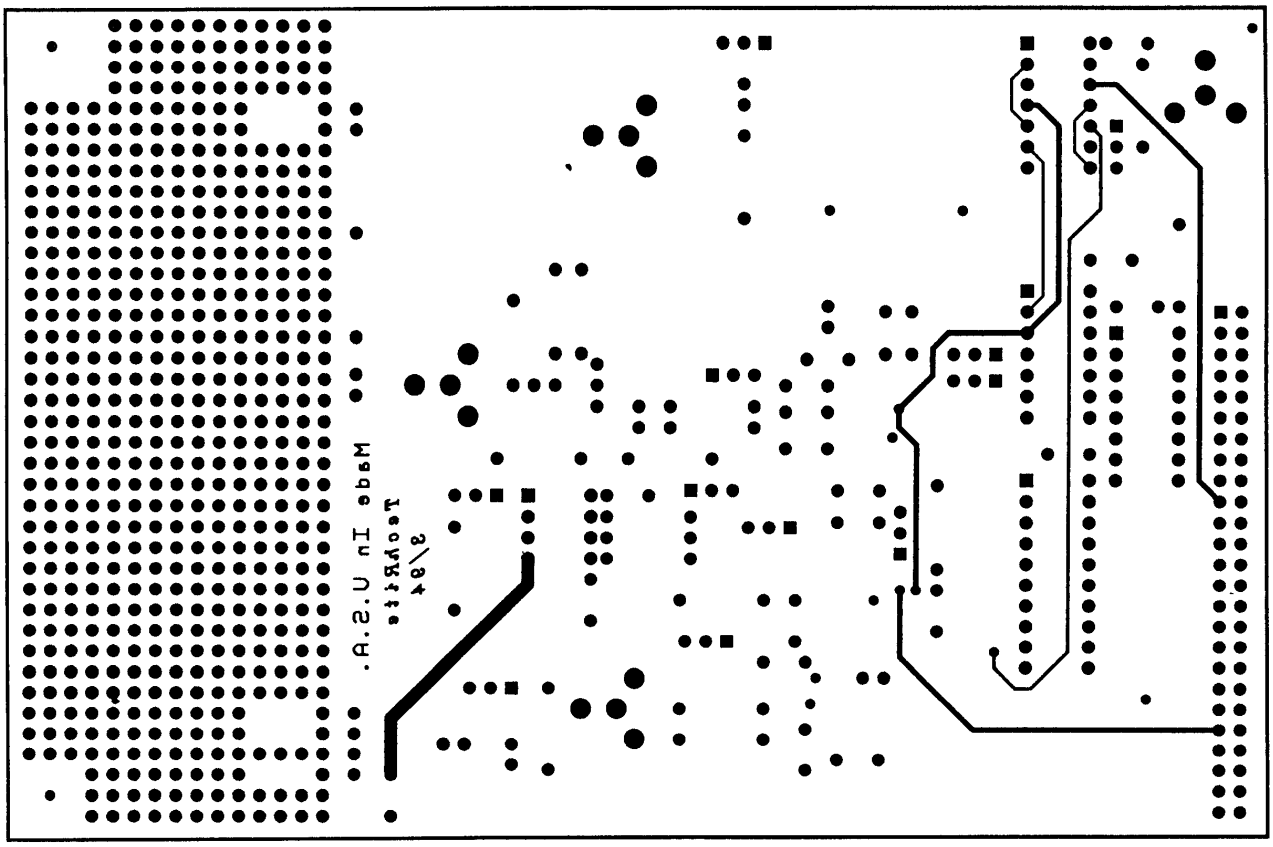


FIGURE 10. SOLDER SIDE

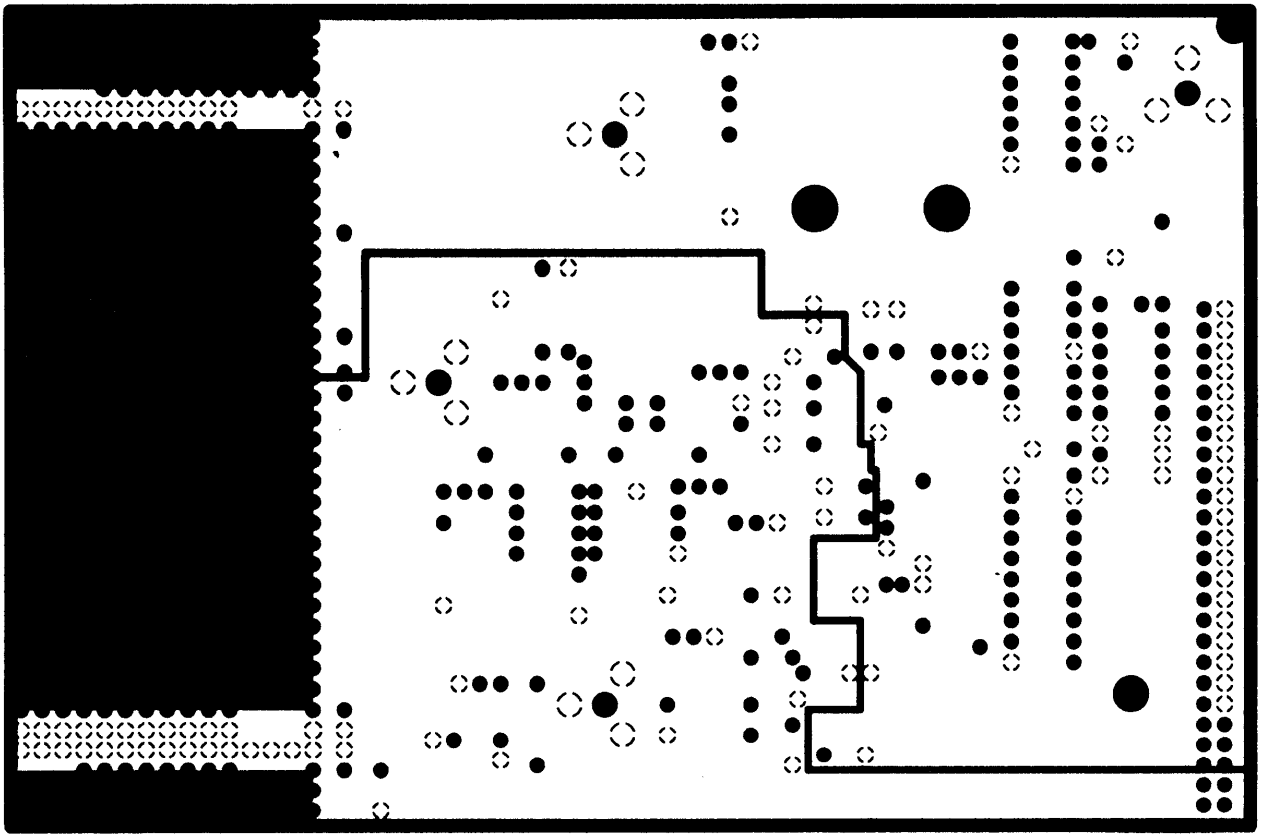


FIGURE 11. GROUND PLANE

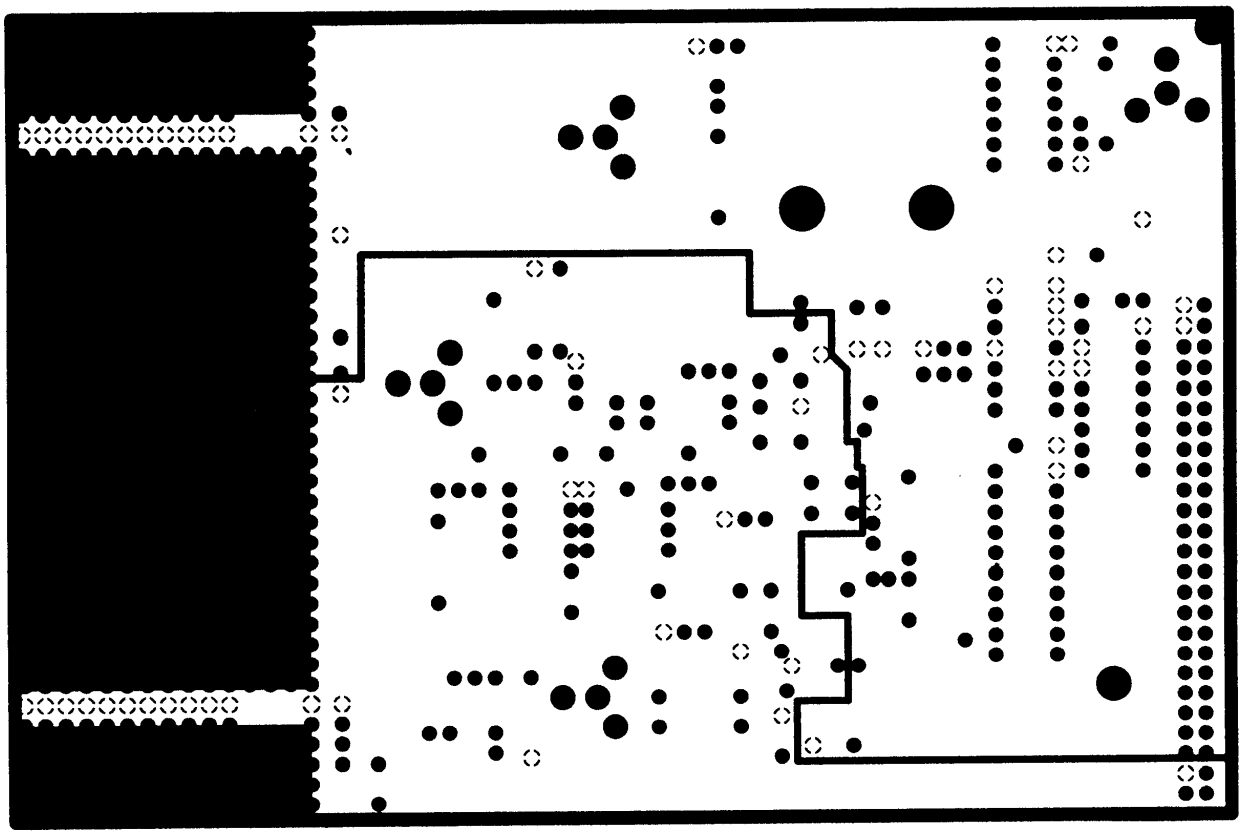


FIGURE 12. POWER PLANE

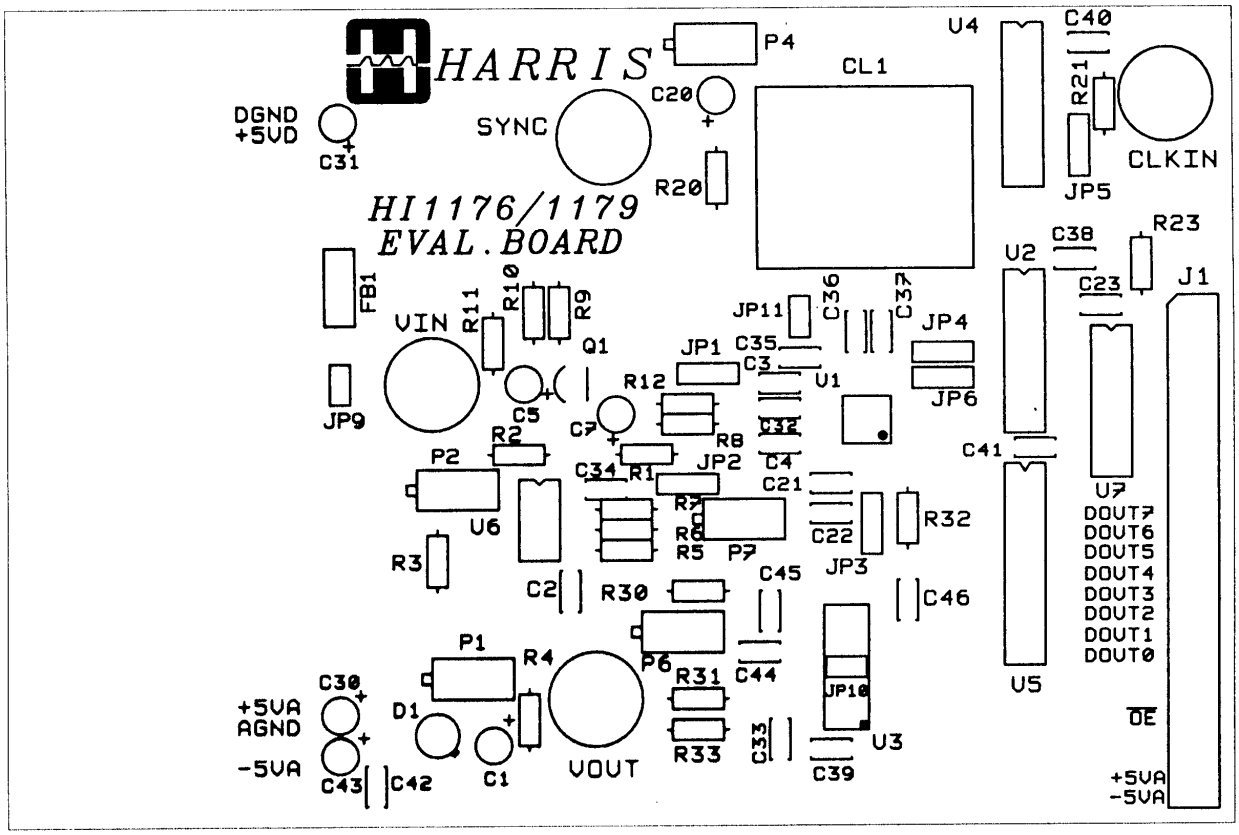


FIGURE 13. SILKSCREEN

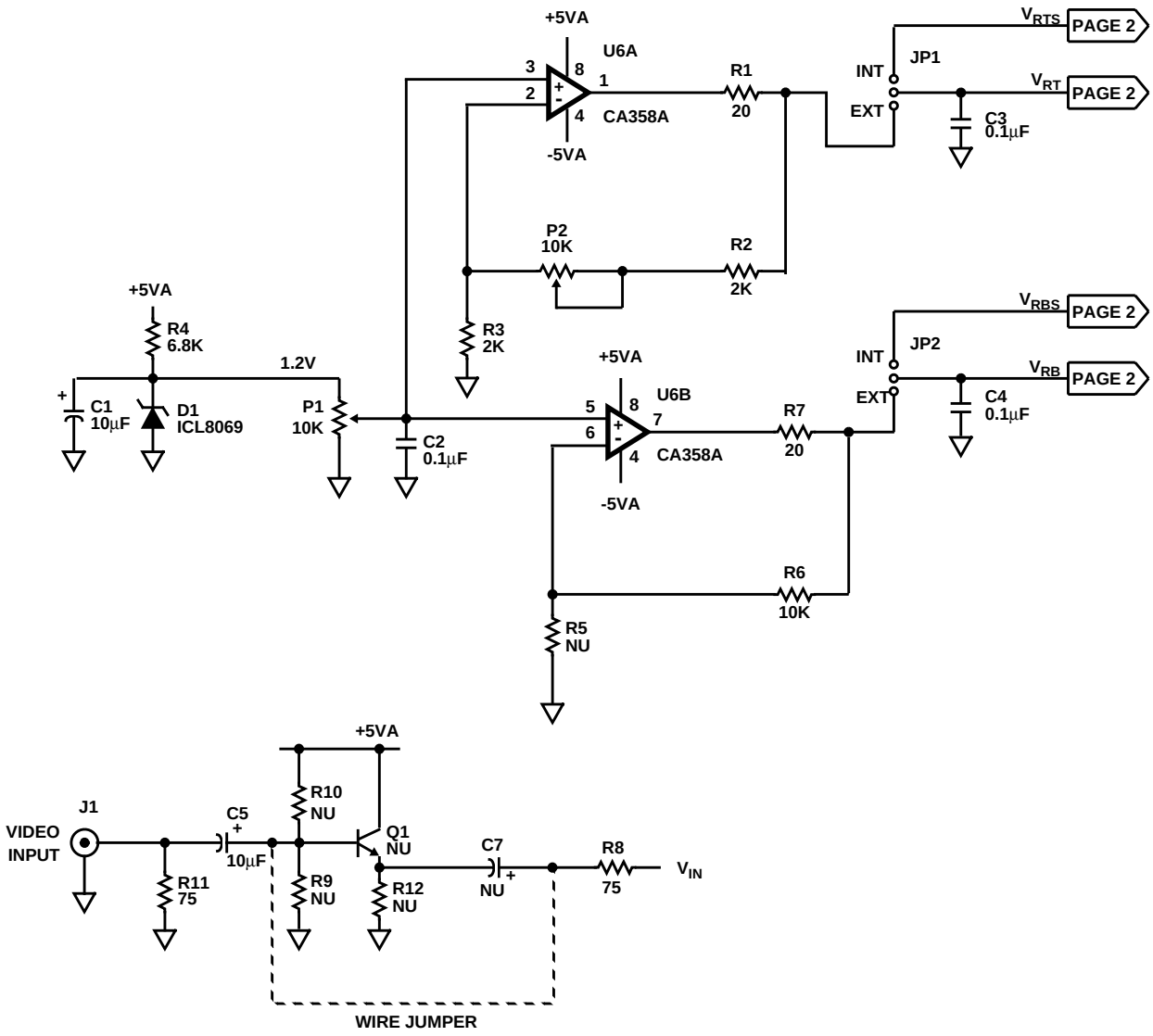


FIGURE 14. SCHEMATIC

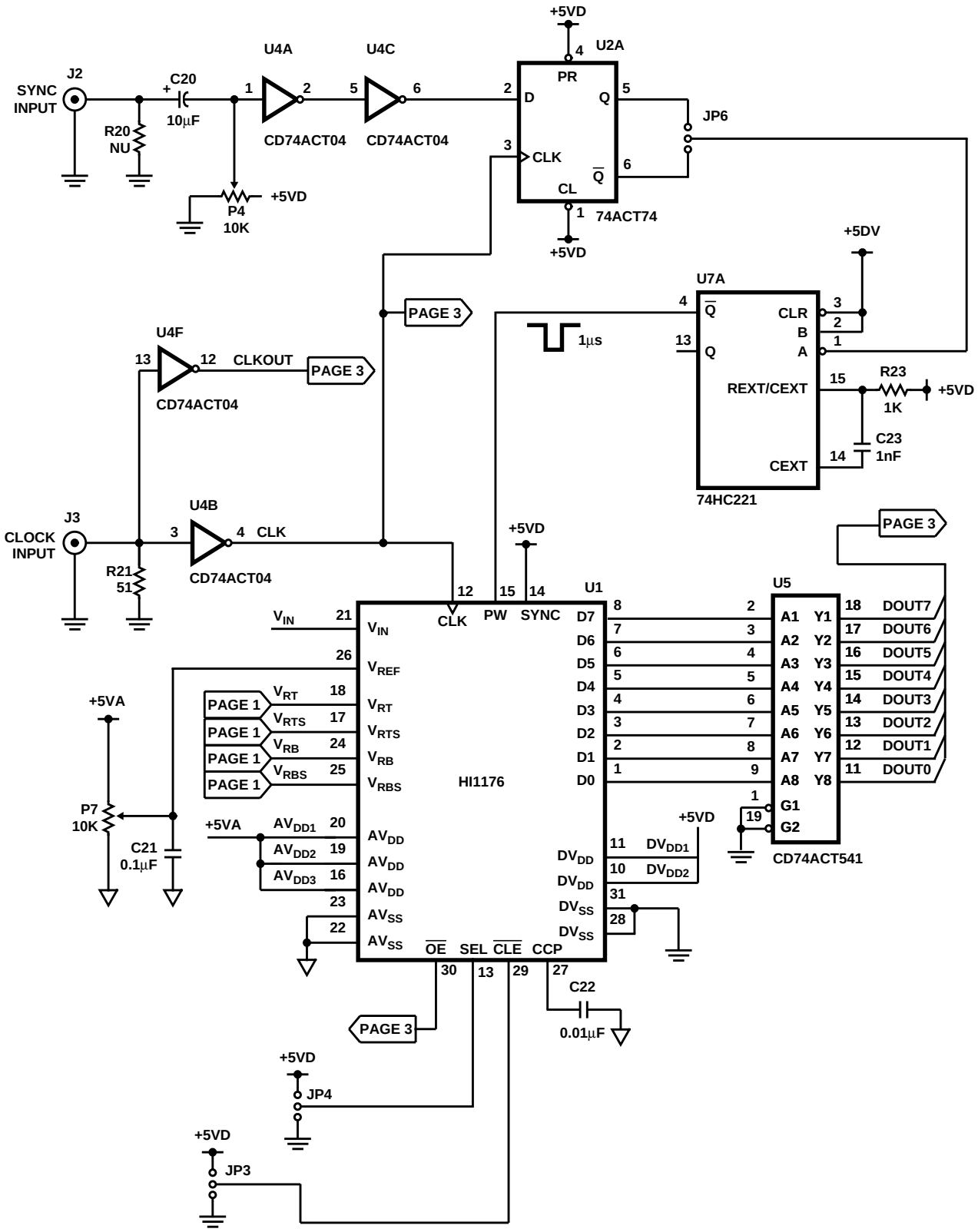


FIGURE 15. SCHEMATIC

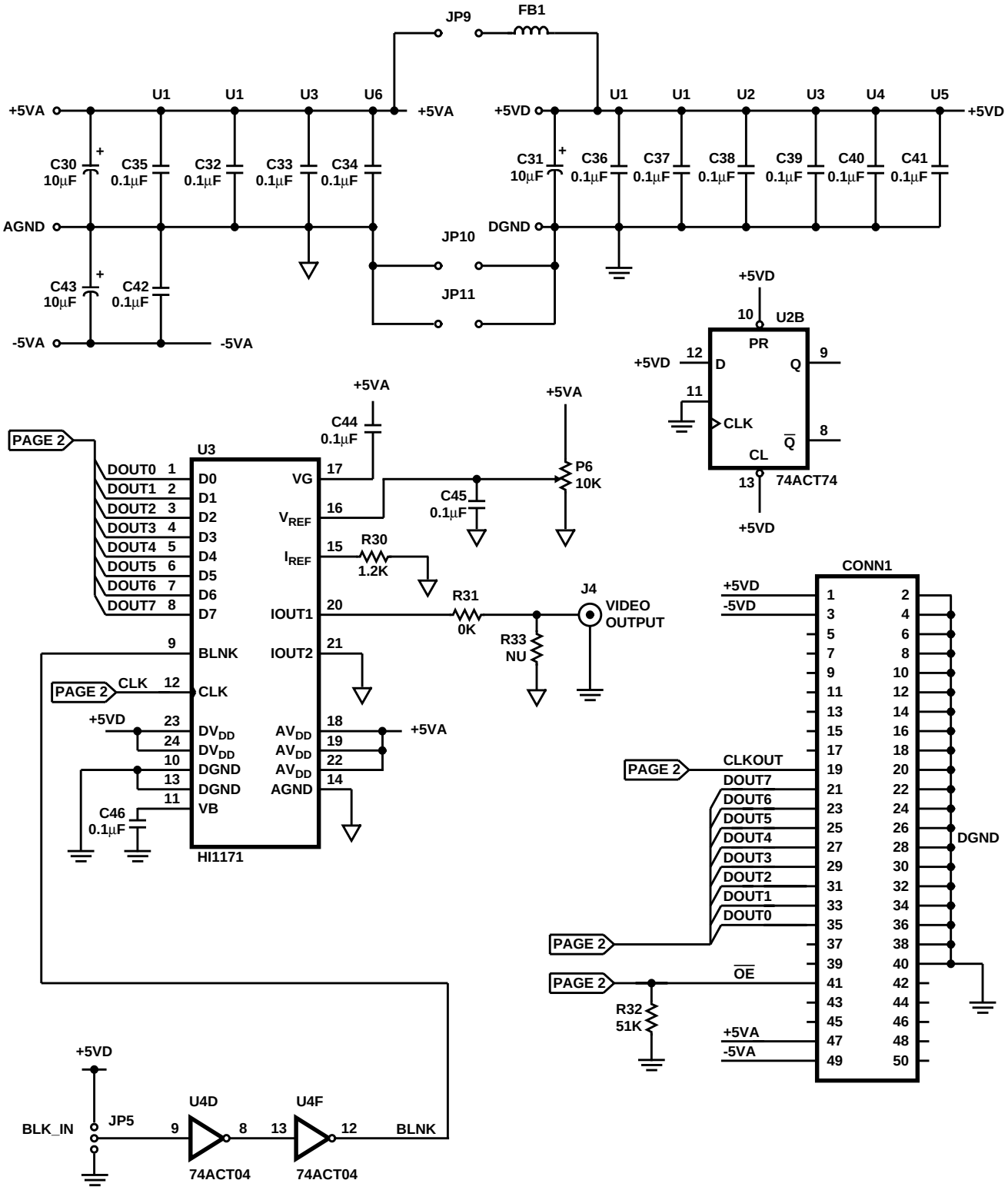


FIGURE 16. SCHEMATIC

RESISTORS 1/8W, 5%	
20	R1, R7
2K	R2, R3
6.8K	R4
10K	R6
75	R8, R11
0(WIRE)	R31
51	R21, R32
1.2K	R30
1K	R23
NU	R5, R9, R10, Ry12, R20, R33
CAPACITORS	
10uF	C1,C5,C20,C30,C31,C43
0.1uF	C2-C4,C21,C32-C42,C44-C46
0.01uF	C22
1nF	C23
NU	C7
ICs	
U1	HI1176 OR HI1179, INTERSIL
U2	CD74ACT74, INTERSIL
U3	HI1171, INTERSIL
U4	CD74ACT04, INTERSIL
U5	CD74ACT541, INTERSIL
U6	CA358A, INTERSIL
U7	CD74HC221, INTERSIL
TRANSISTORS	
NU	Q1
REFERENCES	
D1	ICL8069, INTERSIL

INDUCTORS	
FB1	2743001111, FAIR RITE
POT'S	
10K, 10 TURN, TOP	P1, P2, P4, P6, P7
MISC	
J1-J4	FEMALE BNC CONNECTORS
QTY. 7	SHUNTS (JUMPERS)
JP1-JP6	1X3 HEADER (3 PINS)
JP9	1X2 HEADER (2 PINS)
CONN1	2X25 HEADER (50PINS)
QTY 2	14 PIN LOW PROFILE SOCKET
QTY 1	16 PIN LOW PROFILE SOCKET
QTY 1	20 PIN LOW PROFILE SOCKET
QTY 1	8 PIN LOW PROFILE SOCKET

BUILD NOTES:

1. INSTALL WIRE JUMPER IN JP11.
   LEAVE JP10 OPEN.
2. INSTALL A WIRE JUMPER FOR R31.
3. INSTALL U2, U4, U5, U6, AND U7 IN SOCKETS.
4. INSTALL A WIRE JUMPER FROM C5 TO R8.
   (USE Q1 AND C7 HOLES.)

SETUP NOTES:

1. Set JP1 and JP2 to EXT Position.
   Set P1 to Give 0.5V at VRB EXT.
   Then Set P2 to Give 2.5V at VRT EXT.
2. Set P4 to 2.5V.
3. Set P7 to 1.0V.
4. Set P6 to 1.0V.
5. Install JP1 and JP2 in INT Position.
6. Set JP3 and JP4 in GND Position.
7. Set JP5 in GND Position.
8. Set JP6 to $\overline{Q}$ Output of U2.
9. Verify that U7 PIN 4 has a 1µs Pulse.
10. SYNC Input Must be Connected.

FIGURE 17. PARTS LIST

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**